REMARKS/ARGUMENTS

The Applicants gratefully acknowledge the Examiner's indication of allowably subject matter in claims 16-17.

Reconsideration of the rejected claims is hereby requested.

Recitation of the Invention as-claimed:

In one aspect of the invention, as recited in claim 1, there is provided a method of making a charge-coupled device. In the method, an electrically conducting charge transfer channel is formed in a semiconductor substrate. An electrically insulating layer is formed on a surface of the substrate, and a layer of gate electrode material is formed on the insulating layer.

In accordance with the invention there is formed on the gate material layer a first patterned masking layer having apertures that expose regions of the underlying gate material layer that are to form gate electrodes. The first-pattern-exposed regions of the gate material layer are electrically doped. Further in accordance with the invention a second patterned masking layer is formed on the gate material layer, the second masking layer having apertures that expose regions of the underlying gate material layer that are to form gaps between gate electrodes. The second-pattern-exposed regions of the gate material layer are etched.

The first-pattern-exposed regions of the gate material layer can be electrically doped before the second-pattern-exposed regions of the gate material layer are etched, as recited in claim 4, but such is not in general required, and is not required by the invention as recited in claim 1.

Rejections of the Claims:

Claims 1-6, 12, 14-15, and 18-20 were rejected under 35 U.S.C. §102(b) as being anticipated by Hynecek, U.S. No. 5,972,733 (hereinafter "Hynecek").

To clarify the Hynecek process, the Applicants have attached an enlarged copy of Hynecek Figs. 1 and 2. The Applicants have labeled the identity of each relevant region in these Hynecek figures for the Examiner's reference. Hynecek Fig. 1 shows the finished device structure and Hynecek Fig. 2 shows the structure mid-way through the fabrication sequence.

The Examiner suggested that Hynecek teaches a process in which there is formed an electrically conducting charge transfer channel 24 in a semiconductor substrate 22. The Applicants concur, and Hynecek describes this process: The process begins with a silicon substrate 22 of P-type conductivity. A gate oxide layer 26 is grown and next an N-type buried channel region 24 is formed by N-type doping (Col. 2, lines 15-19). Referring to the Hynecek figures, the substrate 22, buried channel region 24 and oxide layer 26 are identified.

The Examiner suggested that Hynecek teaches a next step of forming an electrically insulating layer 26 on a surface of the substrate 22. As explained above, Hynecek indeed forms an oxide layer 26 on a surface of the substrate 22. This is carried out prior to forming the buried channel region 24 in the substrate.

The Examiner suggested that Hynecek then teaches a step of forming a layer of gate electrode material on the insulating layer 26. The Applicants concur, and Hynecek explains this process: "a layer of polysilicon (semiconductor) 29 is deposited over the oxide layer 26 and doped to be conductive," (Col. 2, lines 19-21).

The Examiner did not identify the gate layer by a reference numeral in the Hynecek figures. The gate layer is the polysilicon layer referred to by Hynecek and is shown as the layer regions 29 in Hynecek Fig. 2, above the oxide layer 26,

not in the substrate, and corresponding to the Hynecek text just referenced. In Hynecek Fig. 1, the gate layer provides the gate regions 28, 30, and 32. Hynecek identifies these as such: "clocked gate regions 28 and 30, antiblooming gate 32," (Col. 2, lines 4-5).

The Examiner suggested that Hynecek teaches forming on the gate layer a first patterned masking layer 70 having apertures that expose regions of the underlying gate material layer that are to form gate electrodes. The Examiner here refers to Hynecek Fig. 1. The Examiner then suggests that Hynecek teaches electrically doping the first-pattern-exposed regions of the gate material layer 24.

The Applicants respectfully submit that the Examiner has here misread Hynecek's description and identification of the gate material layer. The Examiner stated that the gate material layer is identified by reference numeral 24 in the Hynecek figures. This is incorrect. As explained above, reference numeral 24 refers to the buried channel in the substrate 22. Hynecek confirms this: "an N-type buried channel region 24 is formed by N-type doping," (Col. 2, lines 15-19). The gate material is the polysilicon layer regions 29 in Fig. 2 and the polysilicon layer regions 28, 30, 32 in Fig. 1, that are above the substrate, not in the substrate like the buried channel region. The Applicants have identified these regions in the figures for the Examiner.

It thus appears that the Examiner has confused the gate material layer 29 with the buried channel region 24. The gate material layer is above the substrate, over the oxide layer 26. The buried channel region 24 is in the substrate, under the oxide layer 26.

To clarify Hynecek's process, first refer to Hynecek's description with reference to Hynecek Fig. 2. Hynecek explains: A pad oxide layer 70 is grown over the polysilicon layer 29, a nitride layer 72 is deposited on the oxide layer 70, and a TEOS layer 74 is deposited on the nitride layer (Col. 2, lines 26-31). Then

the TEOS layer 74, nitride layer 72, oxide layer 70, and polysilicon gate layer 29 are patterned and etched (Col. 2, lines 31-33). This etch results in apertures which the Applicants have identified in Hynecek Fig. 2.

If Hynecek's oxide layer 70 is to be considered a masking layer as suggested by the Examiner, the apertures formed by etching the oxide layer do not expose regions of the underlying gate material that are to form gate electrodes as suggested by the Examiner and required by the claims. Hynecek etches the gate material 29 along with the TEOS layer 74, nitride layer 72, and oxide layer 70 to expose the oxide-coated substrate below. The oxide layer 70, nitride layer 72, and TEOS layer 74 thus together form a first combination masking layer to protect the gate material layer 29 while the oxide-coated substrate is exposed. Apertures in the patterned combination masking layer 70, 72, 74 do not result in first-pattern-exposed regions of gate material as required by the claims – the apertures expose the oxide layer 26 over the buried channel 24 in the substrate 22. The combination masking layer 70, 72, 74 cover all of the gate material- there is no gate material region exposed through an aperture – see in the Hynecek Figs. 1 and 2 the oxide layer 70, nitride layer 72, and TEOS layer 74 are directly over the gate layer regions; in Fig. 1 the gate regions are identified by reference numerals 28 and 30 and in Fig. 2 the gates are given numeral 29.

Thus, Hynecek etches the gate material layer 29 simultaneously with combination masking layer 70, 72, and 74, so that apertures are formed to expose the oxide-covered buried channel 24, not the gate layer. The apertures are formed by Hynecek to conduct ion implantation steps through the oxide layer into the buried channel region of the substrate: an antiblooming barrier implant 36 is formed in the buried channel 24; then virtual barrier implants 40 and 42 are formed in the buried channel 24; then a clocked barrier implant 46 is formed in the buried channel 24 (Col. 2, lines 35-40). These implantation regions are

formed in the channel 24 in the substrate, not the gate material layer. The Hynecek step of electrical doping of first-pattern-exposed regions referred to by the Examiner is thus doping of the buried channel in the substrate, not the gate material layer as required by the claims.

When does Hynecek electrically dope the gate material layer 29? In direct contradiction with the requirements of the claims, Hynecek electrically dopes the gate material layer when it is first deposited as a blanket layer. As explained above, Hynecek explains: "a layer of polysilicon (semiconductor) 29 is deposited over the oxide layer 26 and doped to be conductive," (Col. 2, lines 19-21). This electrical doping of the blanket polysilicon layer is carried out before the combination masking layer formed of the oxide layer 70, nitride layer 72, and TEOS layer 74 are deposited and all the layers etched with the gate material layer 29. Hynecek does not electrically dope any pattern-exposed regions of the gate material layer as required by the claims; the layer is instead uniformly blanket doped. Hynecek neither teaches nor suggests electrical doping of first-pattern-exposed regions a gate material layer as required by the claims.

The Examiner goes on to suggest that Hynecek teaches forming on the gate material layer a second patterned masking layer 74 having apertures that expose regions of the underlying gate material that are to form gaps between gate electrodes. The Examiner here refers to Hynecek Col. 2, lines 41-67.

The layer 74 referred to here by the Examiner is the TEOS layer 74 described above and shown in Hynecek Fig. 2. As explained above, this is part of the first combination masking layer formed by the oxide layer 70, nitride layer 72, and TEOS layer 74. This <u>first</u> masking layer is formed for protecting the gate material layer regions 29 while regions of the buried channel 24 in the substrate 22 are electrically doped. The masking layer step referred to by the Examiner is formed for electrically doping the substrate, not the gate material layer as required by the claims, and is not formed for etching second-pattern-exposed

regions of the gate material layer as required by the claims. Hynecek neither teaches nor suggests such.

As shown in Hynecek Fig. 2, the etching of the combination masking layer 70, 72, 74 with the gate layer 29 forms apertures that expose the oxide-coated buried channel 24 of the substrate 22. Referring also to Hynecek Fig. 3, Hynecek fills these apertures with polysilicon so that no gaps between gate electrodes are formed with this step. The Hynecek passage referred to by the Examiner describes a process for filing the apertures: "Polysilicon (semiconductor fillings) 76 is then deposited and etched back to fill the regions above the antiblooming barrier implant 36, virtual barrier implants 40, 42, and the clocked barrier implant 46, as shown in Fig. 3," (Col. 2, lines 41-44). Thus, Hynecek's final inter-electrode configuration is not produced by this first masking and doping step as suggested by the Examiner.

The Applicants note that later in the Hynecek process, Hynecek removes some of the gate material layer: "Then the polysilicon regions above the virtual gates [40, 42]...are etched off to form clocked gates 28 and 30...and antiblooming gate 32, as shown in Fig. 5," (Col. 2, lines 53-56). But this step is not conducted with the combination masking layer including the TEOS layer 74 referred to by the Examiner, and none of the oxide layer 70, nitride layer 72, or TEOS layer 74 forms a masking layer for this later step. Hynecek does not teach or specify the masking layer that might be employed here.

The Applicants therefore respectfully submit that Hynecek neither teaches nor suggests the two-step patterned electrical doping and etching process of the invention and required by the claims.

Independent claims 18-20 require the limitations of claim 1 discussed above and missing from the Hynecek process. The Applicants therefore submit

that Hynecek neither teaches nor suggests the methods of independent claims 1, and 18-20.

Claims 2-6, 12, and 14-15 all depend from claim 1 and include all of the requirements of claim 1. As Hynecek is deficient in meeting the requirements of claim 1, so Hynecek is deficient in meeting the requirements of claims 2-6, 12, and 14-15. For clarity, each is discussed in turn below.

Claim 2 requires removing the first patterned masking layer after electrically doping first-pattern-exposed regions of the gate material layer. The Examiner refers to Hynecek Fig. 1 as teaching this required step of the claims. But in Hynecek Fig. 1, there is shown the masking oxide layer 70 over the gate material regions 28 and 30 – this layer is never removed from the device. And as explained above, Hynecek electrically dopes the gate material layer when it is fully exposed before the oxide layer 70 is deposited– Hynecek does not carry out any patterning before the gate material layer is electrically doped as required by the claims. Hynecek dopes the gate material layer 29 without any masking layer in place over the gate material layer 29, and layer 70 is never removed.

Claim 3 requires removing the second patterned masking layer after etching second-pattern-exposed regions of the gate material layer. The Examiner refers to Hynecek Fig. 1 as teaching this required step of the claims. But again, in Hynecek Fig. 1, there is shown the masking oxide layer 70 over the gate regions 28 and 30. As just explained, this oxide remains on the device for operation. Hynecek does not teach or specify a particular masking layer for removing selected polysilicon regions as shown in Hynecek Fig. 5 and explained above.

Claim 4 requires that first-pattern-exposed regions of the gate material layer be electrically doped before the second-pattern exposed regions of the gate material layer are etched. The Examiner here refers again to Hynecek Fig. 1. As

explained above, there is no electrical doping of first-pattern-exposed regions of gate material layer by Hynecek. Hynecek electrically dopes the entire gate material layer, without any pattern in place on the material as required by the claims. As explained above, Hynecek deposits a layer a polysilicon 29 and dopes the layer to be conductive (Col. 2, lines 19-21).

Claim 5 requires that electrical doping of first-pattern-exposed regions of gate material layer be conducted by ion implantation of a selected electrical dopant. As just explained, Hynecek electrically dopes the entire gate material layer, without any pattern in place on the material as required by the claims. For any type of doping process, Hynecek fails to meet the requirements of all the claims that the gate material layer be electrically doped through a first patterned masking layer.

Claim 6 requires that etching of the second-pattern-exposed regions of the gate material layer be conducted by plasma etching. The Examiner here refers to Hynecek Fig. 3. In Hynecek Fig. 3, as discussed above, polysilicon regions 76 are deposited, not etched, to fill in the apertures identified in Fig. 2. It is not clear what in Fig. 3 the Examiner is suggesting would teach plasma etching – the Applicants respectfully submit that there is nothing in Hynecek Fig. 3 that would teach or suggest a step of plasma etching. In fact, there is not even a single mention of plasma etching in the entire Hynecek description.

Claim 12 requires that forming an electrically insulating layer on the substrate surface be carried out by forming a layer of oxide on the substrate surface. As explained above in connection with claim 1, the Applicants concur that Hynecek forms a layer of oxide on a substrate surface. But for any insulating layer material employed, Hynecek fails to meet the requirements of the claims of electrically doping a gate material layer through a first patterned masking layer and etching a gate material layer through a second patterned masking layer.

Claim 14 requires that forming a gate material layer by carried out by depositing a layer of polysilicon on the insulating layer. As explained above in connection with claim 1, the Applicants concur that Hynecek forms a layer of polysilicon on an oxide layer. But for any gate material employed, Hynecek fails to meet the requirements of the claims of electrically doping the gate material layer through a first patterned masking layer and etching the gate material layer through a second patterned masking layer.

Claim 15 requires that the first patterned masking layer and the second patterned masking layer each comprise a layer of photoresist. As explained above and shown in Hynecek Fig. 2, a combination masking layer of oxide 70, nitride 72 and TEOS 74 cover regions of the gate material 29 for electrically doping the buried channel 24. Hynecek neither teaches nor suggests using a layer of photoresist as this masking layer as required by claim 15. Further as explained above, in connection with Hynecek Fig. 5, no photoresist is employed for etching gate electrode regions 28, 30, 32. Hynecek neither teaches nor suggests the use of a photoresist masking layer for such purposes.

Claims 7-11 and 13 were rejected under 35 U.S.C. §103(a) as being obvious over Hynecek, U.S. No. 5,972,733 (hereinafter "Hynecek") in view of Rhodes, U.S. No. 4,742,016 (hereinafter "Rhodes") and further in view of Erhardt, U.S. No. 5,114,833 (hereinafter "Erhardt").

Claim 7 requires heat treating the electrically-doped and etched gate material to diffuse electrical dopant through the gate material layer thickness. Claim 8 requires that the heat treating be annealing. Claim 9 further requires that the heat treating be oxidation of the gate material layer. Claim 10 further requires that first and second masking layers each have a pattern of apertures that are characterized by an extent which accounts for lateral dopant diffusion during heat treatment.

The Examiner suggested that Hynecek teaches all of the requirements of claims 7, 8, 9, and 10 except the required heat treatments.

The Examiner referred to Rhodes Col. 5, lines 4-27 as teaching the requirements of claims 7-10. At this Rhodes passage there is described "a high temperature step used to diffuse the arsenic implanted in the first oxide layer out into the underlying silicon," (Col. 5, lines 4-6). This step is directed to the doping of the substrate, not a gate material layer, by diffusing dopant from an oxide layer atop the substrate into the substrate itself. No teaching or even suggestion of using this step for diffusing dopant through a gate material is given. Instead, Rhodes requires that the heat treating be a tailored annealing step to "minimize problems arising from variation of channel potentials in the storage region of the first-phase set of electrodes," (Col. 5, lines 8-10). The storage region of the substrate is defined by an ion implantation doping step and the resulting storage region is indicated by ++++ signs and reference numeral 31 in the substrate in Fig. 4. The annealing referred to in Col. 5 results in doped substrate regions indicated by ++++ signs and reference numeral 30 in the substrate in Fig. 6. Nothing more can be implied from this process as Rhodes explicitly requires it to be tailored for defining the substrate doping, not gate material layer doping.

Claim 9 requires that the heat treating be oxidation of the gate material layer. The heat treating technique of Rhodes described at Rhodes Col. 5 above does not teach or even suggest oxidizing gate material. It is solely directed to diffusing dopant out of an oxide layer 21 into the underlying substrate 20 as shown in Fig. 6. The description is simply devoid of any suggestion for a gate material layer oxidation technique.

Claim 9 further requires that the heat treating be oxidation of the gate material layer. The heat treating technique of Rhodes described at Rhodes Col. 5 does not teach or even suggest oxidizing gate material. It is solely directed to diffusing dopant out of an oxide layer 21 into the underlying substrate 20 as

shown in Fig. 6. The description is simply devoid of a suggestion for a gate oxidation technique.

Claim 10 further requires that first and second masking layers each have a pattern of apertures that are characterized by an extent which accounts for lateral dopant diffusion during heat treatment. This is shown in Fig. 4D of the instant application and described at Page 14, lines 20+ of the instant application. In Fig. 4D there is shown a gate material layer 18 which has been selectively doped to form doped regions 42, the edges of which are indicated with dotted lines. A second patterned masking layer of photoresist 40 is shown atop of the gate layer. As explained in the instant application, the photoresist regions 44 that shield the doped gate layer regions 42 preferably extend beyond the edges of the doped gate layer regions to account for subsequent lateral dopant diffusion.

The Examiner referred to Col. 4, lines 20-57 and Col. 5, lines 4-27 to Rhodes as teaching such. The Applicants submit that nowhere in Rhodes is there shown or even suggested an arrangement of mask aperture extent that accounts for lateral dopant diffusion as required by claim 10. Rhodes blanket dopes a gate material layer exactly in the manner of Hynecek, and etches such in the conventional fashion. As a result, Rhodes has absolutely no concern with lateral diffusion through a gate material layer. Even if the oxide-to-substrate dopant diffusion step at Rhodes Col. 5 were to be considered a gate electrode annealing step, at that point the gate electrode is already etched and therefore it would be nonsensical for Rhodes to consider lateral gate electrode diffusion at that step.

Claim 11 requires that the forming of an electrically conducting charge transfer channel in a semiconductor substrate comprise ion implantation of a selected electrical dopant into the substrate.

In Rhodes Fig. 4 and Col. 4, lines 20-35, there is taught a masking layer 26 used to selectively dope the substrate, as explained in detail above. Beginning at

Col. 4, line 19, Rhodes explains that the "storage region" of the substrate is defined by this ion implantation doping step and the resulting substrate doping is indicated by ++++ signs and reference numeral 31 in the substrate in Fig. 4. Therefore Rhodes does teach the use of ion implantation into a substrate. But as explained above, this ion implantation step is indeed directed to forming a charge transfer channel in the substrate and is not directed to doping of a gate electrode layer. Hynecek is completely silent as to the technique he employs for doping a buried channel, Hynecek states simply "an N type buried channel region 24 is formed by N type doping," (Col. 2, lines 18-19). For any dopant step employed by Erhardt, and any charge transfer channel formation technique, all of Hynecek, Rhodes, and Erhardt fail to teach or suggest the first-pattern-exposed gate material layer doping and second-pattern-exposed gate layer etching steps required by all of the claims.

Claim 13 requires that the gate material be deposited as a layer of amorphous silicon. The Examiner refers to Erhardt here, but the Examiner does not actually cite any figure or passage in Erhardt that teaches the use of amorphous silicon. None of Hynecek, Erhardt, or Rhodes teach or suggest the use of amorphous silicon. They all employ polysilicon: Erhardt at Col. 2, lines 40-41 specifies "polysilicon gate electrodes 20 and 22." Rhodes uses "gate electrodes 24, advantageously of polysilicon, as is usual in such devices," (Col. 4, lines 5-6). As explained above, Hynecek says likewise: "a layer of polysilicon 29 is deposited over the oxide layer 26," (Col. 2, lines 20-21). None of Hynecek, Erhardt, or Rhodes, nor any combination of the three, teach or suggest the use of amorphous silicon as a gate electrode material, and there is no obvious design choice to be made here; polysilicon is the conventional choice for gate electrode material.

None of Hynecek, Erhardt, or Rhodes, considered alone or in any combination, teach or suggest requirements of the claims. The Applicants

respectfully submit that the claims are in condition for allowance, which action is requested.

If the Examiner has any questions or would like to discuss the claims, he is encouraged to telephone the undersigned Agent directly at his convenience at the phone number given below.

Respectfully submitted,

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